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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,944	04/21/2004	Gregory J. Smith	50019.276US01/P05838	7191

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EXAMINER	
LAXTON, GARY L	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 09/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/828,944	SMITH, GREGORY J.	
	Examiner	Art Unit	
	Gary L. Laxton	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations of claims 11, 12 and 15-17 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an

application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 24 and 26 are objected to because of the following informalities:

Claims 24 and 26 recite "associated with control signal" [sic].

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 3, 6-8 and 13-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites the limitation "the resistor circuit" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 3 is also vague and confusing. First of all, characters in parentheses are generally ignored and not given any patentable weight. Therefore, applicant's formula in claim 3 line 7, does not have meaning since the variables are not defined. Secondly, applicant seems to be confusing the resistors R_{FB1} and R_{SNS}. Applicant recites a sense circuit comprising a resistor

coupled between a reference terminal and a sense terminal. Both R_{FB1} and R_{SNS} reside between a reference terminal (ground or Vref) and a sense terminal (V_X or Diode "D"). However, applicant mentions the reference value is "Vref". Therefore, just when one assumes the applicant is referring to R_{FB1} in claim 3 line 2, applicant then recites that the resistor has a resistance value R_{SNS}. So which resistor is the applicant referring to? And what exactly does applicant mean by "I_{SNS}*R_{SNS}", since neither variable is defined. The examiner assumes applicant is referring to resistor R_{FB1} in the claim.

Claims 6-8 inherit the same deficiencies as claim 3.

Claim 13 recites "arranged to bias signal" [sic]. It is unclear what applicant is trying to claim in this instance. Claims 14-20 inherit the same from claim 13.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 2, 9-12, 21-23 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Tateishi (US 5,912,552).

Tateishi disclose a switched mode power converter that is arranged to provide an output signal to a load circuit, the switched mode power converter comprising: an inductor (L); a switching circuit (Q1, Q2 et al) that is coupled to the inductor and arranged to periodically energize the inductor in response to a control signal (FF1), wherein the switching circuit is

operated in: a closed circuit position during a first operating phase of the converter, and an open circuit position during a second operating phase of the converter; a sense circuit (Rs) that is arranged to provide a sense signal that is related to a current in the inductor during a selected operating phase of the converter, wherein the selected operating phase corresponds to one of the first and second operating phases of the converter, and wherein a non-selected operating phase of the converter corresponds to the other of the first and second operating phases of the converter; a feedback circuit (V_{FB}) that is arranged to provide a feedback signal in response to an output signal of the converter; a comparator circuit (56) that is arranged to assert a start signal when the feedback signal and the sense signal are approximately equal during the selected operating phase of the converter; and a one-shot circuit (62) that is arranged to initiate the control signal when the start signal is asserted such that the control signal has a variable pulse-width during the non-selected operating phase of the converter (Abstract).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tateishi (US 5,912,552) in view of Littlefield (US 5,959,443)

Claims 3-6; Tateishi discloses the claimed subject matter in regards to claim 1 supra, except for a sense circuit that comprises a first resistor that is coupled between a switching

circuit and a supply terminal, a trans-conductance circuit that is arranged to provide a sense current to a sense terminal in response to a voltage across the first resistor, and a second resistor that is coupled between a reference voltage and the sense terminal such that the sense signal corresponds to a voltage associated with the sense terminal.

Littlefield teaches a sense circuit that comprises a first resistor (103) that is coupled between a switching circuit (101) and a supply terminal (ground), a trans-conductance circuit (400) that is arranged to provide a sense current to a sense terminal (VIl) in response to a voltage across the first resistor (Rs), and a second resistor (407: R1) that is coupled between a reference voltage (ground) and the sense terminal (VIL) such that the sense signal corresponds to a voltage associated with the sense terminal in order to effect improvements in efficiency and output ripple.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Tateishi to include a sense circuit that comprises a first resistor that is coupled between a switching circuit and a supply terminal, a trans-conductance circuit that is arranged to provide a sense current to a sense terminal in response to a voltage across the first resistor, and a second resistor that is coupled between a reference voltage and the sense terminal such that the sense signal corresponds to a voltage associated with the sense terminal in order to effect improvements in efficiency and output ripple as taught by Littlefield.

Claim 7; Diode D2 of Tateishi.

Claim 8; bandgap circuits are well known reference voltage circuits. Thus, it would have been obvious to use a bandgap circuit to provide a stable reference voltage to the circuit.

10. Claims 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tateishi (US 5,912,552) in view of Szepesi (US 4,535,399).

Tateishi discloses the claimed subject matter in regards to claims 23 and 25 supra, except for adjusting a pulse width associated with a control signal during a selected operating phase of the converter with a phase locked loop.

Szepesi teaches using a PLL to adjust a pulse width from a pulse width modulation circuit by forcing the circuit to initiate the modulating pulses at the load current zero crossing in order to control the flow of energy from the power source to a tuned load.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Tateishi to include adjust a pulse width associated with a control signal during a selected operating phase of the converter with a phase locked loop in order to force the circuit to initiate the modulating pulses at the load current zero crossing in order to control the flow of energy from the power source to a tuned load as taught by Szepesi.

Allowable Subject Matter

11. Claims 13-20 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

Claims 13-20; the examiner considers these claims to contain allowable subject matter despite the 112 2nd paragraph issues noted above; since prior art fails to disclose or suggest, inter alia, a switched mode power converter comprising a PLL circuit that is arranged to bias the control signal based on a comparison between a reference frequency and a feedback frequency that is associated with the control signal.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 6,580,258 Wilcox et al disclose a control circuit and method for maintaining high efficiency in a regulator circuit; US 6,064,187 Redl et al discloses a voltage regulator compensation circuit and method.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary L. Laxton whose telephone number is (571) 272-2079. The examiner can normally be reached on Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gary L. Laxton
Primary Examiner
Art Unit 2838

8/31/05